PM100CBS060

FLAT-BASE TYPE
INSULATED PACKAGE

PM100CBS060

FEATURE

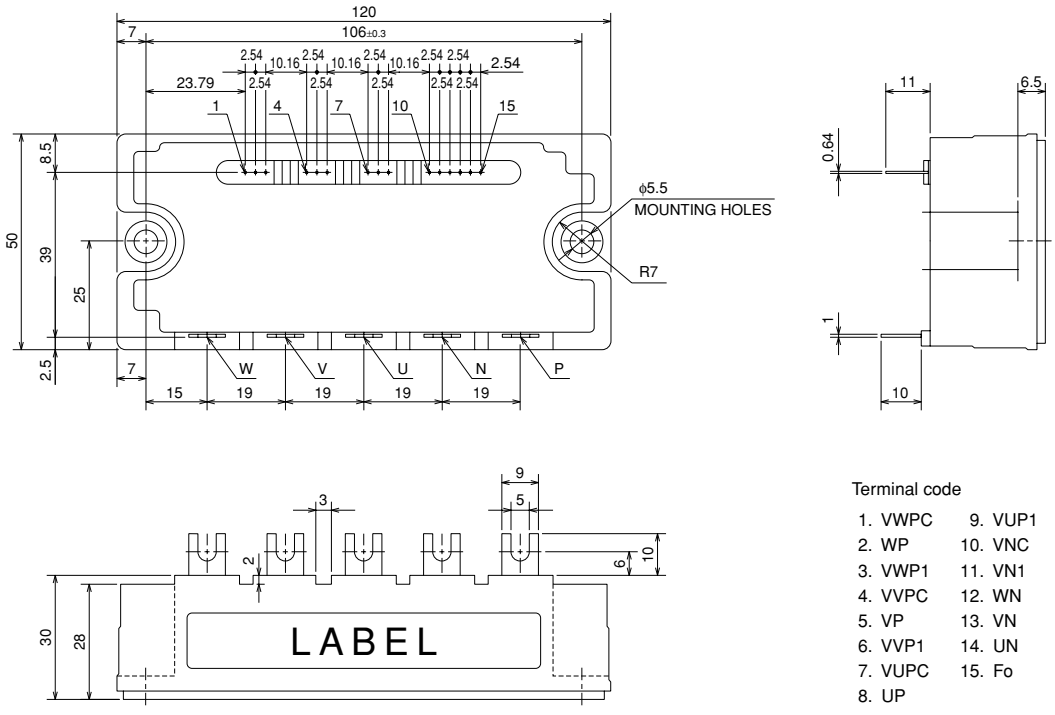
a) Adopting 4th generation IGBT chip, which performance is improved by 1μm fine rule process.
For example, typical Vce(sat)=1.7V
b) Using new Diode which is designed to get soft reverse recovery characteristics.
c) Over-temperature protection by detecting T_j of the IGBT chips

- 3ϕ 100A, 600V Current-sense IGBT type inverter
- Monolithic gate drive & protection logic
- Detection, protection & status indication circuits for over-current, short-circuit, over-temperature & under-voltage
- Acoustic noise-less 11kW class inverter application

APPLICATION

Servo drives and other motor controls

PACKAGE OUTLINES **Dimensions in mm**



Terminal code

1. VWPC	9. VUP1
2. WP	10. VNC
3. VWP1	11. VN1
4. VVPC	12. WN
5. VP	13. VN
6. VVP1	14. UN
7. VUPC	15. Fo
8. UP	

MITSUBISHI ELECTRIC

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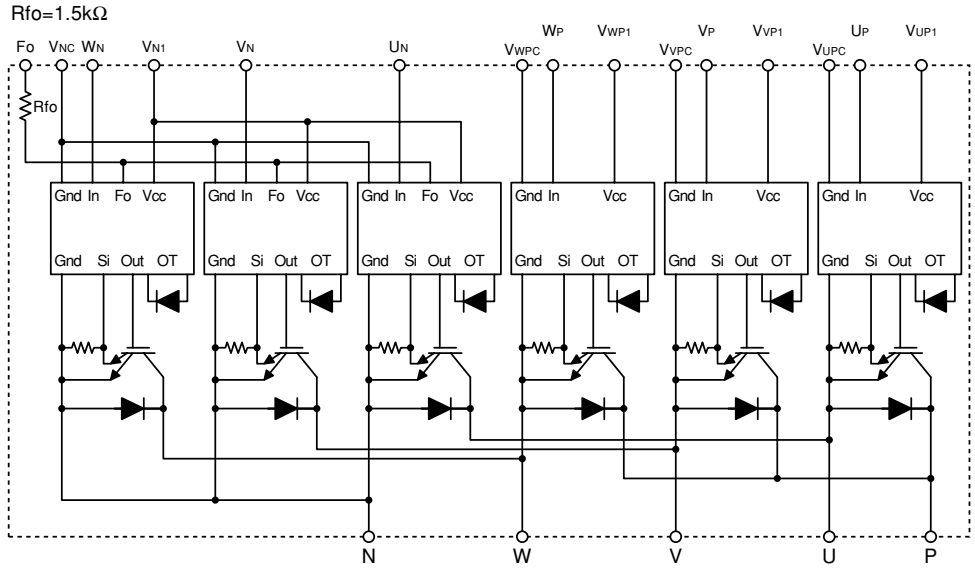
INTERNAL FUNCTIONS BLOCK DIAGRAM



MAXIMUM RATINGS (Tj = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Conditions	Ratings	Unit
V_{CES}	Collector-Emitter Voltage	V_D = 15V, V_{CIN} = 15V	600	V
±I_C	Collector Current	T_C = 25°C	100	A
±I_{CP}	Collector Current (Peak)	T_C = 25°C	200	A
P_C	Collector Dissipation	T_C = 25°C	568	W
T_j	Junction Temperature		–20 ~ +150	°C

CONTROL PART

Symbol	Parameter	Conditions	Ratings	Unit
V_D	Supply Voltage	Applied between : V_{UP1}-V_{UPC}, V_{VP1}-V_{VPC}, V_{WP1}-V_{WPC}, V_{N1}-V_{NC}	20	V
V_{CIN}	Input Voltage	Applied between : U_P-V_{UPC}, V_P-V_{VPC}, W_P-V_{WPC}, U_N • V_N • W_N-V_{NC}	20	V
V_{FO}	Fault Output Supply Voltage	Applied between : F_O-V_{NC}	V_D+0.5	V
I_{FO}	Fault Output Current	Sink current at F_O terminal	20	mA

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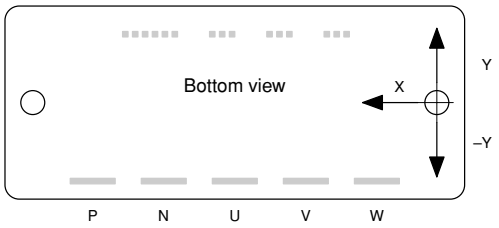
TOTAL SYSTEM

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC(PROT)}$	Supply Voltage Protected by OC & SC	V_D = 13.5 ~ 16.5V, Inverter Part, T_j = 125°C Start	400	V
$V_{CC(surge)}$	Supply Voltage (Surge)	Applied between : P-N, Surge value	500	V
T_C	Module Case Operating Temperature	(Note-1)	–20 ~ +110	°C
T_{stg}	Storage Temperature		–40 ~ +125	°C
V_{iso}	Isolation Voltage	60Hz, Sinusoidal Charged part to Base, AC 1 min.	2500	V_{rms}

(Note-1) Tc(under the chip) measurement point is below.

(Unit : mm)

Arm / Axis	U_P		V_P		W_P		U_N		V_N		W_N	
	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi
X	83.3	83.3	41.8	41.8	16.8	16.8	70.8	70.8	54.3	54.3	29.3	29.3
Y	4.9	–4.8	4.9	–4.8	4.9	–4.8	–1.2	–10.8	–1.2	–10.8	–1.2	–10.8



THERMAL RESISTANCES

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c')Q}$	Junction to case Thermal Resistances	Tc measured point is just under the chips Inverter IGBT part (per 1/6 module)	—	—	0.22*	°C/W
$R_{th(j-c')F}$		Tc measured point is just under the chips Inverter FWDi part (per 1/6 module)	—	—	0.36*	°C/W
$R_{th(c-f)}$	Contact Thermal Resistance	Case to fin, (per 1 module) Thermal grease applied	—	—	0.046	°C/W

*: If you use this value, $R_{th(f-a)}$ should be measured just under the chips.

ELECTRICAL CHARACTERISTICS (Tj = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Test Conditions		Limits			Unit
				Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	V_D = 15V, I_C = 100A, V_{CIN} = 0V, Pulsed (Fig. 1)	T_j = 25°C	—	1.7	2.3	V
			T_j = 125°C	—	1.7	2.3	
V_{EC}	FWDi Forward Voltage	–I_C = 100A, V_D = 15V, V_{CIN} = 15V (Fig. 2)		—	2.2	3.3	V
t_{on}	Switching Time	V_D = 15V, V_{CIN} = 15V↔0V, V_{CC} = 300V, I_C = 100A, T_j = 125°C, Inductive Load (Fig. 3)		0.8	1.2	2.4	µs
t_{rr}				—	0.15	0.3	µs
$t_{c(on)}$				—	0.4	1.0	µs
t_{off}				—	2.4	3.3	µs
$t_{c(off)}$				—	0.5	1.0	µs
I_{CES}	Collector-Emitter Cutoff Current	V_{CE} = V_{CES}, V_D = 15V (Fig. 4)	T_j = 25°C	—	—	1	mA
			T_j = 125°C	—	—	10	

CONTROL PART

Symbol	Parameter	Test Conditions		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit Current	V_D = 15V, V_{CIN} = 15V	V_{N1}-V_{NC}	—	40	60	mA
			V_{XP1}-V_{XPC}	—	13	18	
$V_{th(ON)}$	Input ON Threshold Voltage	Applied between : U_P-V_{UPC}, V_P-V_{VPC}, W_P-V_{WPC}		1.2	1.5	1.8	V
$V_{th(OFF)}$	Input OFF Threshold Voltage	U_N • V_N • W_N-V_{NC}		1.7	2.0	2.3	V
OC	Over Current Trip Level	V_D = 15V (Fig. 5,6)	T_j = –20°C	—	—	470	A
			T_j = 25°C	220	290	390	
			T_j = 125°C	158	—	—	
SC	Short Circuit Trip Level	–20≤ T_j ≤ 125°C, V_D = 15V (Fig. 5,6)		—	360	—	A
$t_{off(OC)}$	Over Current Delay Time	V_D = 15V (Fig. 5,6)		—	10	—	µs
OT	Over Temperature protection	Detect T_j of IGBT chip	Trip level	135	145	155	°C
OT_r			Reset level	—	125	—	°C
UV	Supply Circuit Under-Voltage Protection	–20 ≤ T_j ≤ 125°C	Trip level	11.5	12.0	12.5	V
UV_r			Reset level	—	12.5	—	V
$I_{FO(H)}$	Fault Output Current	V_D = 15V, V_{FO} = 15V (Note-2)		—	—	0.01	mA
$I_{FO(L)}$				—	10	15	mA
t_{FO}	Minimum Fault Output Pulse Width	V_D = 15V (Note-2)		1.0	1.8	—	ms

(Note-2) Fault output is given only when the internal OC, SC, OT & UV protection.
Fault output of OC, SC, OT & UV protection operate by lower arm.
Fault output of OC, SC protection given pulse.
Fault output of OT, UV protection given pulse while over trip level.

MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Main terminal screw : M5	2.5	3.0	3.5	N • m
—	Mounting torque	Mounting part screw : M5	2.5	3.0	3.5	N • m
—	Weight	—	—	400	—	g

RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Test Conditions	Recommended value	Unit
V_{CC}	Supply Voltage	Applied across P-N terminals	≤ 400	V
V_D	Control Supply Voltage	Applied between : U_{UP1}-V_{UPC}, V_{VP1}-V_{VPC} V_{WP1}-V_{WPC}, V_{N1}-V_{NC} (Note-3)	15.0 ± 1.5	V
$V_{CIN(ON)}$	Input ON Voltage	Applied between : U_P-V_{UPC}, V_P-V_{VPC}, W_P-V_{WPC}	≤ 0.8	V
$V_{CIN(OFF)}$	Input OFF Voltage	U_N • V_N • W_N-V_{NC}	≥ 4.0	V
f_{PWM}	PWM Input Frequency	Using Application Circuit of Fig.8	≤ 20	kHz
t_{dead}	Arm Shoot-through Blocking Time	For IPM's each input signals (Fig. 7)	≥ 2.5	µs

(Note-3) With ripple satisfying the following conditions
dv/dt swing ≤ ±5V/µs, Variation ≤ 2V peak to peak

PRECAUTIONS FOR TESTING

1. Before appling any control supply voltage (V_D), the input terminals should be pulled up by resistores, etc. to their corresponding supply voltage and each input signal should be kept off state.
   After this, the specified ON and OFF level setting for each input signal should be done.
2. When performing “OC” and “SC” tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
   (These test should not be done by using a curve tracer or its equivalent.)

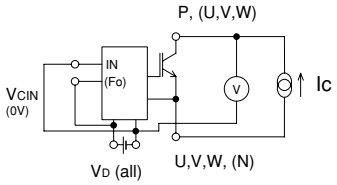


Fig. 1 $V_{CE(sat)}$ Test

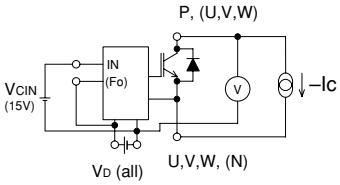


Fig. 2 V_{EC} Test

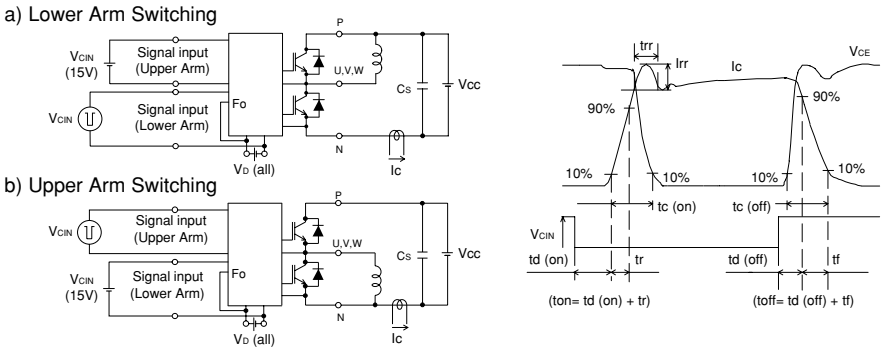


Fig. 3 Switching time Test circuit and waveform

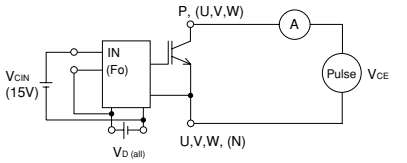


Fig. 4 I_{CES} Test

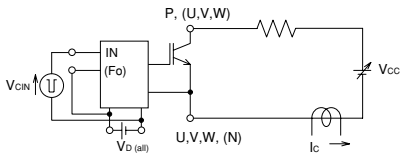


Fig. 5 OC and SC Test

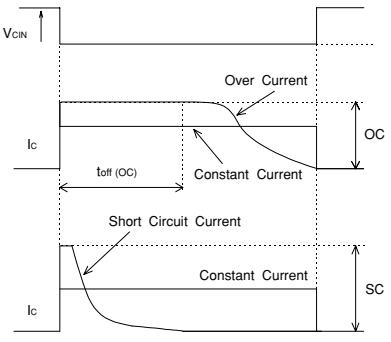


Fig. 6 OC and SC Test waveform

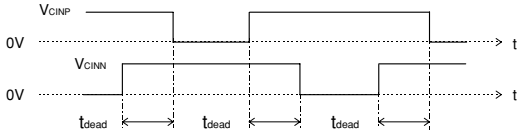


Fig. 7 Dead time measurement point example

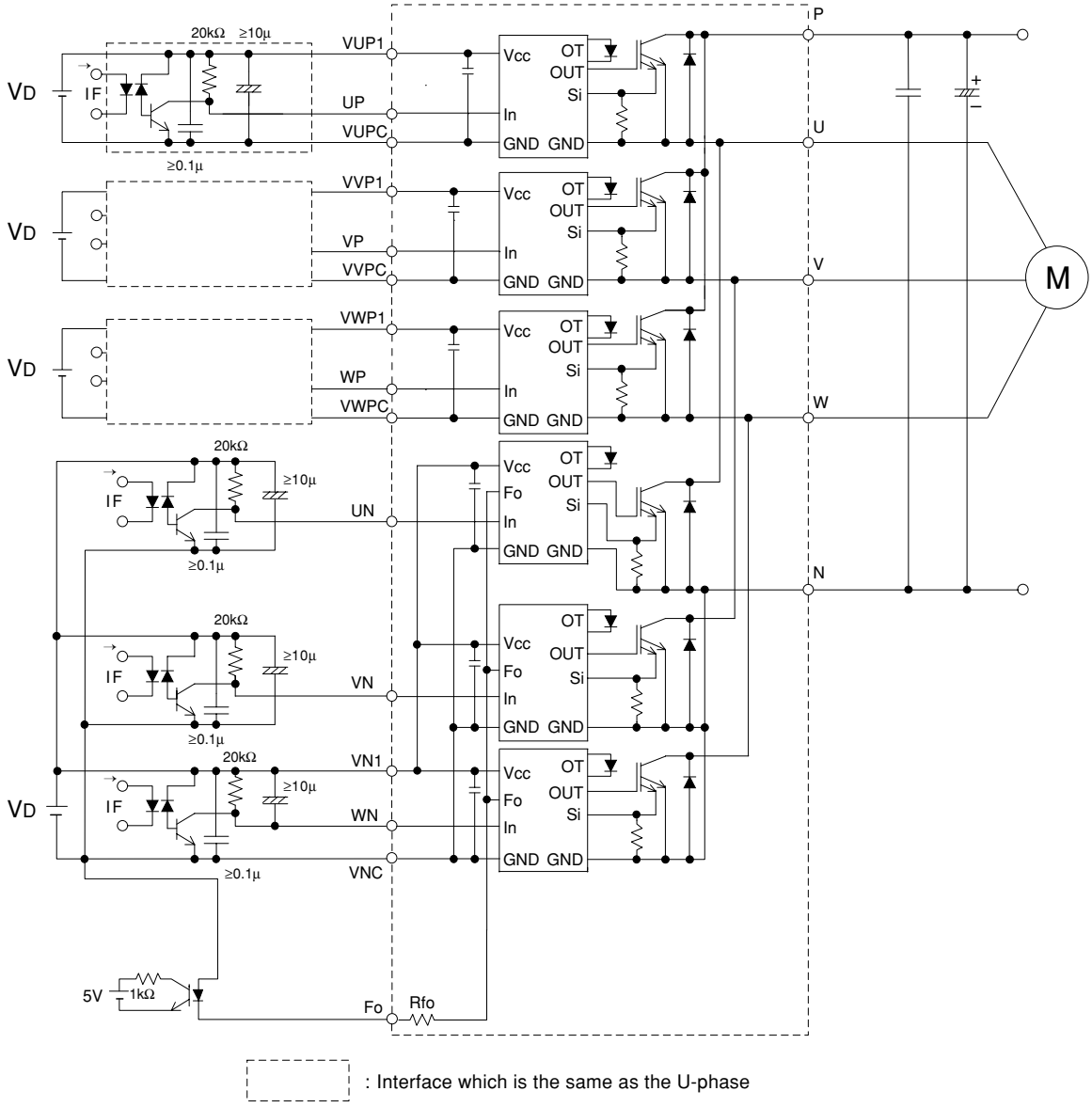


Fig. 8 Application Example Circuit

NOTES FOR STABLE AND SAFE OPERATION ;

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers : t_{PLH}, $t_{PHL} \leq 0.8\mu s$, Use High CMR type.
- Slow switching opto-coupler : CTR > 100%
- Use 4 isolated control power supplies (V_D). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.